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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,315	03/29/2001	Fumitoshi Karube	1163-0330P	1861
2292	7590	11/12/2004	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747				REKSTAD, ERICK J
ART UNIT		PAPER NUMBER		
		2613		

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/820,315	KARUBE ET AL.
	Examiner	Art Unit
	Erick Rekstad	2613

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 6/29/2004.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-3 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 29 March 2001 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This is a final rejection for application no. 09/820,315 in response to the amendment filed on June 29, 2004.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5,926,208 to Noonan et al in view of US Patent 6,434,196 to Sethuraman et al, "Video DSP Architecture for MPEG2 CODEC" by T. Araki et al and US Patent 6,038,5800 to Yeh.

[claim 1]

As shown in Figure 3, Noonan teaches an image processing device (Multimedia Encode Processor) comprising a video processor (1038), a VLC (262), external data interface (214), instruction memory (152, 222, 224, and 226) and a processor means (1038) for decoding the instruction held by said instruction memory, and for performing a programmed control operation on said video processor, VLC processor, and external data interface means (Col 7 Lines 48-58, Col 8 Lines 1-45 and 56-67, Col 9 Lines1-15, Fig. 2 and 3). Noonan does not teach the use of SIMD calculating means for performing operations, such as motion compensation, motion prediction, DCT processing, IDCT processing, quantization, and reverse quantization by means of a

pipeline operation unit that can be program controlled by an outside unit. Noonan further does not teach the VLC processor performing variable-length decoding.

As shown in Figure 1 and 14B, Sethuraman teaches an image processing device (100, Fig. 1) comprising an SIMD calculating means (1400, Fig. 14B) for performing operations, such as motion compensation, motion prediction, DCT processing, IDCT processing, quantization, and reverse quantization by means of a pipeline operation unit that can be program controlled by an outside unit in order to process multiple macroblocks at the same time with a single instruction stream (Col 34 Lines 40-45 and Lines 54-67, Col 35 Lines 1-9 and Lines 20-41, Figs. 1, 14A and 14B). Sethuraman does not teach a VLC performing variable-length decoding. Sethuraman further does not teach the DCT and IDCT units are integrated. It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the video processor of Noonan with the SIMD processor of Sethuraman in order to process multiple macroblocks at the same time with a single instruction stream.

Araki teaches the use of a VLC/VLD processor with a VPCU in an image processor in order to flexibly support the specifications of MPEG1, MPEG2, as well as other standards (Page II-418 Second column Second paragraph, Fig. 2). Araki teaches the use of a DCT/IDCT unit combined with vector processing units to execute parallel vector operations in SIMD scheme (Page II-418 Section 3.1, Fig. 2). Araki does not specifically teach the DCT/IDCT in said SIMD calculating means. It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the VLC of Noonan with the VLC/VLD of Araki in order to flexibly support multiple video formats.

As shown above Sethuraman teaches the SIMD processing unit of Figure 14B. The figure shows the DCT and IDCT as separate modules. Sethuramn further teaches that the modules need not be isolated into separate modules (Col 35 Lines 42-45). Yeh teaches a DCT/IDCT unit which uses SIMD to provide a lower hardware cost and modular design suitable for VLSI implementation (Col 2 Lines 35-41, Col 5 Lines 13-25 and Lines 42-46, Fig. 6). It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the separate DCT and IDCT modules of Sethuramn with the DCT/IDCT unit of Yeh in order to provide a lower hardware cost and modular design suitable for VLSI implementation.

[claims 2 and 3]

Noonen teaches the image processing device wherein said instruction memory is a RAM (Col 8 Lines 65-67, Fig. 3). Noonen further teaches the instructions stored in ROM (1052) (Col 7 Lines 13-18, Col 10 Lines 64-67, Fig. 2A).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erick Rekstad whose telephone number is 703-305-5543. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 703-305-4856. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2613

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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